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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/770,479	02/04/2004	Masaki Ito	NITT.0189	1890
7590	12/30/2005		EXAMINER	
REED SMITH LLP Suite 1400 3110 Fairview Park Drive Falls Church, VA 22042			THOMPSON, ANNETTE M	
			ART UNIT	PAPER NUMBER
			2825	

DATE MAILED: 12/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 18 October 2005 has been entered.
2. Applicant's amendment to 10/770,479 has been examined and remarks carefully reviewed. Claims 6 and 7 are cancelled. Claims 1 and 4 are amended. Claims 1-5 are pending.
3. Applicant's amendment and remarks have been reviewed and are considered persuasive. Claims 1-5 contain allowable subject matter.

Priority

4. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 06/06/2001. It is noted, however, that applicant has not filed a certified copy of the foreign application as required by 35 U.S.C. 119(b). Examiner has reviewed the contents of the parent application, 10/083,341, and the certified copy is not present as part of the contents.

Specification

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Allowable Subject Matter

6. Claims 1-5 are allowed over the prior art of record.
7. The following is an examiner's statement of reasons for allowance: In a design method of a semiconductor integrated circuit device, the prior art does not teach an interface checker integrated into the semiconductor integrated circuit device so as to form one simulation model.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

8. This application is in condition for allowance except for the following formal matters: Applicant must provide a title that is relevant to the subject matter of Applicant's claims.

Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

Any inquiry concerning this communication or earlier communications should be directed to Examiner A.M. Thompson whose telephone number is (571) 272-1909. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 4:30 p.m..

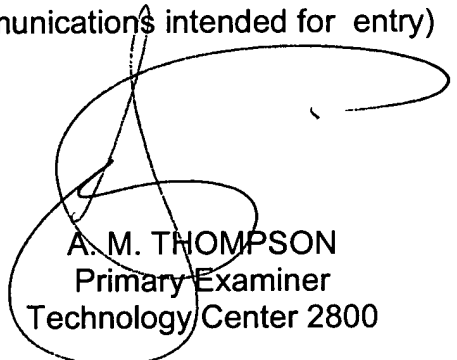
9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

10. Responses to this action should be mailed to the appropriate mail stop:

Mail Stop _____
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or faxed to:

(571) 273-8300, (for all **OFFICIAL** communications intended for entry)



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